Amendments to the Claims

Please amend the claims in the manner indicated.

1. (cancelled)

2. (currently amended) ~~The VCO of claim 1,~~ A voltage controlled oscillator (VCO) comprising:

a first PMOS device having a strained-silicon layer;

wherein the first PMOS device comprises a source region, a drain region, a gate region and a body; and

wherein the body is coupled to a bias voltage source to increase buried channel conduction within at least the first PMOS device so as to reduce flicker noise within the VCO.

3. (currently amended) ~~The VCO of claim 1, further~~ A voltage controlled oscillator (VCO) comprising:

a first PMOS device having a strained-silicon layer;

a second PMOS device having a strained-silicon layer and cross-coupled to the first PMOS device.

4. (Original) The VCO of claim 3, wherein the first PMOS device comprises a first source region, a first drain region, a first gate region and a first body;

wherein the second PMOS device comprises a second source region, a second drain region, a second gate region and a second body; and

wherein the second gate region is coupled to the first drain region and the second drain region is coupled to the first gate region.

5. (Original) The VCO of claim 4, wherein the first and second bodies are coupled to a first bias voltage source to increase buried channel conduction within the first and second PMOS devices so as to reduce flicker noise within the VCO.

6. (Original) The VCO of claim 5, further comprising:

a third PMOS device having a strained-silicon layer, a third source region, a third drain region, a third gate region and a third body, the third PMOS device to provide a tail-current source to the VCO.

7. (Original) The VCO of claim 6, wherein first, second and third bodies are coupled to a first bias voltage source to increase buried channel conduction within the first, second and third PMOS devices so as to reduce flicker noise within the VCO.

8. (currently amended) The VCO of claim 6, wherein the third gate region ~~of the third PMOS device~~ is coupled to a second bias voltage source to control the tail current through the third PMOS device.

9. (currently amended) The VCO of claim 6, further comprising at least one inductive element and at least one capacitive element each coupled between the first drain region ~~a drain of the first PMOS device~~ and the second drain region ~~a drain of the second PMOS device~~.

10. (Original) A voltage controlled oscillator (VCO) comprising:

at least a first strained-silicon PMOS device having a first source, a first drain, a first gate and a first body; and

a control bias coupled to the first body to increase buried channel conduction within the first PMOS device so as to reduce flicker noise within the VCO.

11. (Original) The VCO of claim 10, further comprising:

a second strained-silicon PMOS device having a second source, a second drain, a second gate and a second body; and

a third strained-silicon PMOS device having a third source, a third drain, a third gate and a third body;

wherein the control bias is coupled to the second and third bodies to increase buried channel conduction within the second and third respective PMOS devices so as to further reduce flicker noise within the VCO.

12. (Original) The VCO of claim 11, wherein the second gate is coupled to the first drain and the second drain is coupled to the first gate.

13. (Original) The VCO of claim 12, further comprising a second control bias coupled to the third strained-silicon PMOS device to modulate tail-current through the third strained-silicon PMOS device.

14. (currently amended) The VCO of claim 13, further comprising at least one inductive element and at least one capacitive element each coupled between [[a]] the first drain ~~of the first PMOS device~~ and [[a]] the second drain ~~of the second PMOS device~~.

15. (currently amended) A system comprising:

a communication channel;

a dynamic random access memory (DRAM) ~~DRAM~~; and

an integrated circuit (IC) coupled to the DRAM via the communication channel, the IC having a phase locked loop (PLL) to generate an output clock signal, the PLL including

a voltage controlled oscillator (VCO) comprising

at least a first strained-silicon PMOS device having a first gate, a first drain, and a first body terminal, and

a control bias coupled to the first body terminal ~~of the strained-silicon PMOS device~~ to increase buried channel conduction within the ~~respective~~ first strained-silicon PMOS device[[s]] so as to reduce flicker noise within the VCO.

16. (currently amended) The VCO of claim 15, further comprising:

a second strained-silicon PMOS device having ~~a source,~~ a second drain, a second gate and a second body terminal, wherein the second gate is coupled to the first drain and the second drain is coupled to the first gate.

17. (Original) The system according to claim 15, wherein the integrated circuit further includes a central processing unit, a main memory coupled to the central processor unit and at least one input/output module coupled to the central processor unit and the main memory.

18. (currently amended) The system of claim 15, wherein the integrated circuit [[is]] comprises a microprocessor.

19. (Original) The system of claim 15, further comprising a networking interface coupled to the communication channel.

20. (currently amended) The system of claim 15, wherein the system [[is]] comprises a selected one of a set-top box, an entertainment unit and a DVD player.